PL620-20

Low Phase Noise XO (for HF Fund. and 3rd O.T.)

FEATURES

- 100MHz to 200MHz Fund. or 3rd OT Crystal.
- Output range: 100 – 200MHz (no multiplication).
- Available outputs: PECL, or LVDS.
- OESEL/OECTRL for both PECL & LVDS.
- Supports 2.5V or 3.3V-Power Supply.
- Available in die form.
- Die thickness 10 mil.

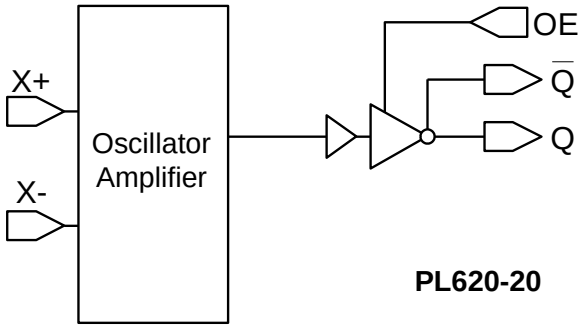
DESCRIPTION

The PL620-20 is an XO IC specifically designed to work with high frequency fundamental and third overtone crystals. Its design was optimized to tolerate higher limits of interelectrode capacitance and bonding capacitance to improve yield. It achieves very low current into the crystal resulting in better overall stability. It is ideal for XO applications requiring LVDS or PECL output levels at high frequencies.

DIE SPECIFICATIONS

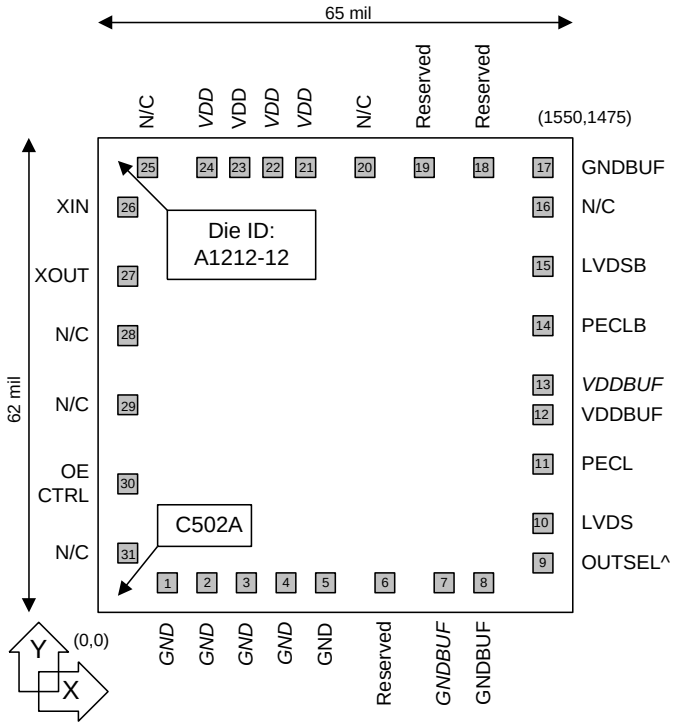
Name	Value
Size	62 x 65 mil
Reverse side	GND
Pad dimensions	80 micron x 80 micron
Thickness	10 mil

BLOCK DIAGRAM



PL620-20

DIE CONFIGURATION



OUTPUT SELECTION AND ENABLE

Pad #9 OUTSEL	Selected Output
0	LVDS
1	PECL (default)

Pad #9 OUTSEL	Pad #30 OE_CTRL	State
0	0	Tri-state
	1	Output enabled (default)
1	0	Output enabled (default)
	1	Tri-state

Pad #9: Bond to GND to set to "0", bond to VDD to set to "1"
Pad #30: Logical states defined by PECL levels if OUTSEL is "1"
Logical states defined by CMOS levels if OUTSEL is "0"

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, dc	V_I	-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*	T_A	-40	85	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

* **Note**: Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

2. Crystal Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Resonator Frequency	F_{XIN}	Fundamental or 3rd overtone*	100		200	MHz
Crystal Loading Rating	$C_{L\ (xtal)}$	Die only		3.0		pF
Interelectrode Capacitance	C_0				3	pF
Recommended ESR	R_E	F_{XIN}<160MHz and C0<3.0pF			30	Ω
		F_{XIN}<200MHz and C0<3.0pF			25	Ω
		F_{XIN}<200MHz and C0<2.5pF			30	Ω

* **Note**: 3rd overtone crystals require an external resistor between XIN and XOUT to prevent the fundamental from oscillating.

3. General Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current (Loaded Outputs)	I_{DD}	PECL/LVDS			100/80	mA
Operating Voltage	V_{DD}		2.25		3.63	V
Output Clock Duty Cycle		@ 1.25V (LVDS) @ V_{DD} – 1.3V (PECL)	45 45	50 50	55 55	%
Short Circuit Current				±50		mA

4. Jitter Specifications

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Period jitter RMS at 155MHz	At 155.52MHz, with capacitive decoupling between VDD and GND. Over 10,000 cycles		2.5		ps
Period jitter peak-to-peak at 155MHz			18.5	20	
Accumulated jitter RMS at 155MHz	At 155.52MHz, with capacitive decoupling between VDD and GND. Over 1,000,000 cycles.		2.5		ps
Accumulated jitter peak-to-peak at 155MHz			24	27	
Random Jitter	"RJ" measured on Wavecrest SIA 3000		2.5		ps
Integrated jitter RMS at 155MHz	Integrated 12 kHz to 20 MHz		0.3	0.4	ps

Note: Higher Q factor of 3rd overtone crystals will result in even better jitter performance.

5. Phase Noise Specifications

PARAMETERS	FREQUENCY	@10Hz	@100Hz	@1kHz	@10kHz	@100kHz	UNITS
Phase Noise relative to carrier	155.52MHz	-75	-95	-125	-140	-145	dBc/Hz

Note: Higher Q factor of 3rd overtone crystals will result in even better phase noise performance.

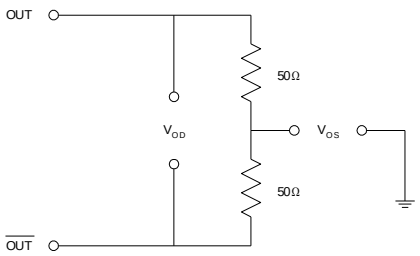
6. LVDS Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Differential Voltage	V_{OD}	R_L = 100 Ω (see figure)	247	355	454	mV
V_{DD} Magnitude Change	ΔV_{OD}		-50		50	mV
Output High Voltage	V_{OH}			1.4	1.6	V
Output Low Voltage	V_{OL}		0.9	1.1		V
Offset Voltage	V_{OS}		1.125	1.2	1.375	V
Offset Magnitude Change	ΔV_{OS}		0	3	25	mV
Power-off Leakage	I_{OXD}	V_{out} = V_{DD} or GND, V_{DD} = 0V		±1	±10	uA
Output Short Circuit Current	I_{OSD}			-5.7	-8	mA

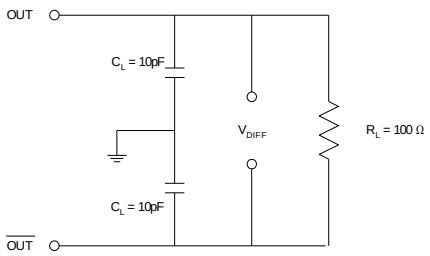
7. LVDS Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Clock Rise Time	t_r	R_L = 100 Ω, C_L = 10 pF (see figure)	0.2	0.7	1.0	ns
Differential Clock Fall Time	t_f		0.2	0.7	1.0	ns

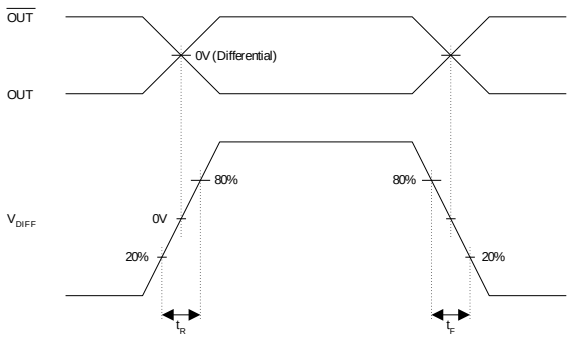
LVDS Levels Test Circuit



LVDS Switching Test Circuit



LVDS Transistion Time Waveform



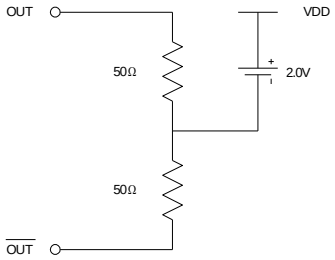
8. PECL Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	MAX.	UNITS
Output High Voltage	V_{OH}	R_L = 50 Ω to (V_{DD} – 2V) (see figure)	V_{DD} – 1.025		V
Output Low Voltage	V_{OL}			V_{DD} – 1.620	V

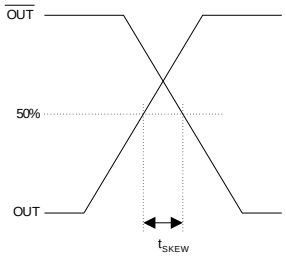
9. PECL Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Clock Rise Time	t_r	@20/80% - PECL		0.6	1.5	ns
Clock Fall Time	t_f	@80/20% - PECL		0.5	1.5	ns

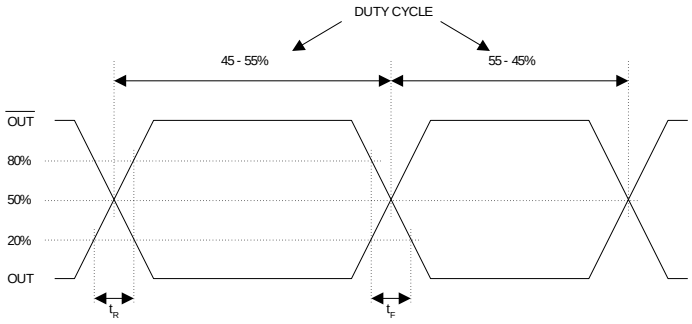
PECL Levels Test Circuit



PECL Output Skew



PECL Transistion Time Waveform



PAD ASSIGNMENT

Pad #	Name	X (µm)	Y (µm)	Description
1	*Optional GND*	248	109	Optional Ground.
2	*Optional GND*	361	109	Optional Ground.
3	*Optional GND*	473	109	Optional Ground.
4	*Optional GND*	587	109	Optional Ground.
5	GND	702	109	Ground.
6	*Reserved*	874	109	Reserved for future use.
7	*Optional GNDBUF*	1042	109	Optional Ground, buffer circuitry.
8	GNDBUF	1171	109	Ground, buffer circuitry.
9	OUTSEL	1400	125	Output type selector. Internal pull up. See Output Selection and Enable table on page 1. Internal pull up.
10	LVDS	1400	259	LVDS output.
11	PECL	1400	476	PECL output.
12	VDDBUF	1400	616	3.3V power supply, buffer circuitry.
13	*Optional VDDBUF*	1400	716	Optional 3.3V power supply, buffer circuitry.
14	PECLB	1400	871	Complementary PECL output.
15	LVDSB	1400	1089	Complementary LVDS output.
16	*Not connected*	1400	1227	Not Connected.
17	GNDBUF	1389	1365	Ground, buffer circuitry.
18	*Reserved*	1232	1365	Reserved for future use.
19	*Reserved*	1042	1365	Reserved for future use.
20	*Not connected*	854	1365	Not Connected.
21	*Optional VDD*	659	1365	Optional 3.3V power supply.
22	*Optional VDD*	559	1365	Optional 3.3V power supply.
23	VDD	459	1365	3.3V power supply.
24	*Optional VDD*	358	1365	Optional 3.3V power supply.
25	*Not connected*	194	1365	Not Connected.
26	XIN	109	1223	Crystal input. See Crystal Specifications on page 2.
27	XOUT	109	1017	Crystal output. See Crystal Specifications on page 2.
28	*Not connected*	109	858	Not Connected.
29	*Not connected*	109	646	Not Connected.
30	OE_CTRL	109	397	Used to enable/disable the output(s). See Output Selection and Enable table on page 1.
31	*Not connected*	109	181	Not Connected.

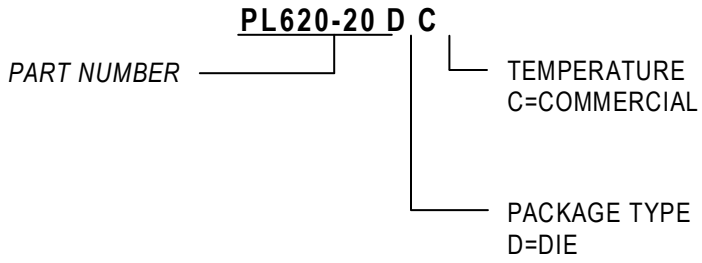
Note: for optimal Phase Noise performance, it is recommended to bond all optional VDD and GND pads.

ORDERING INFORMATION

For part ordering, please contact our Sales Department:
2180 Fortune Drive, San Jose, CA 95131, USA
Tel: (408) 944-0800 Fax: (408) 474-1000

PART NUMBER

The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range



Order Number	Marking	Package Option
PL620-20DC	P620-20DC	Die – Waffle Pack

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